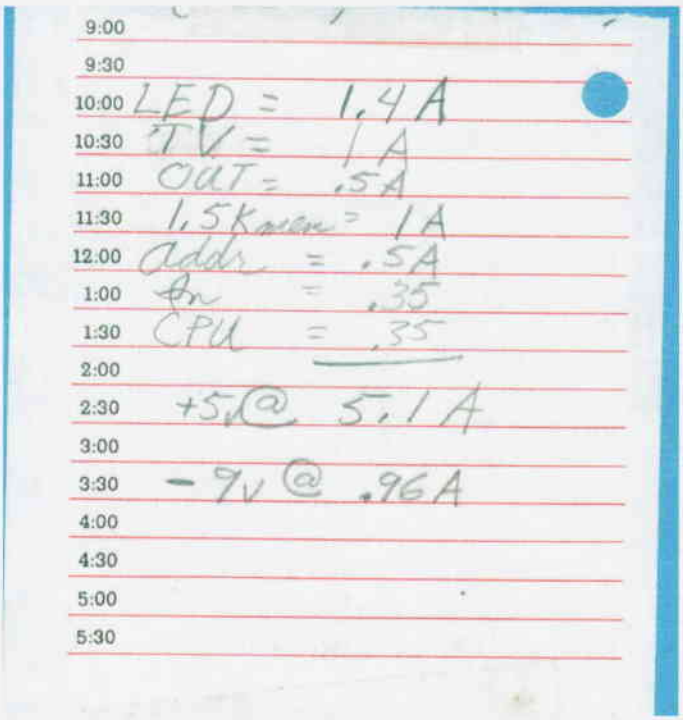
Documents from Dr. Robert Sudings Personal Notebook



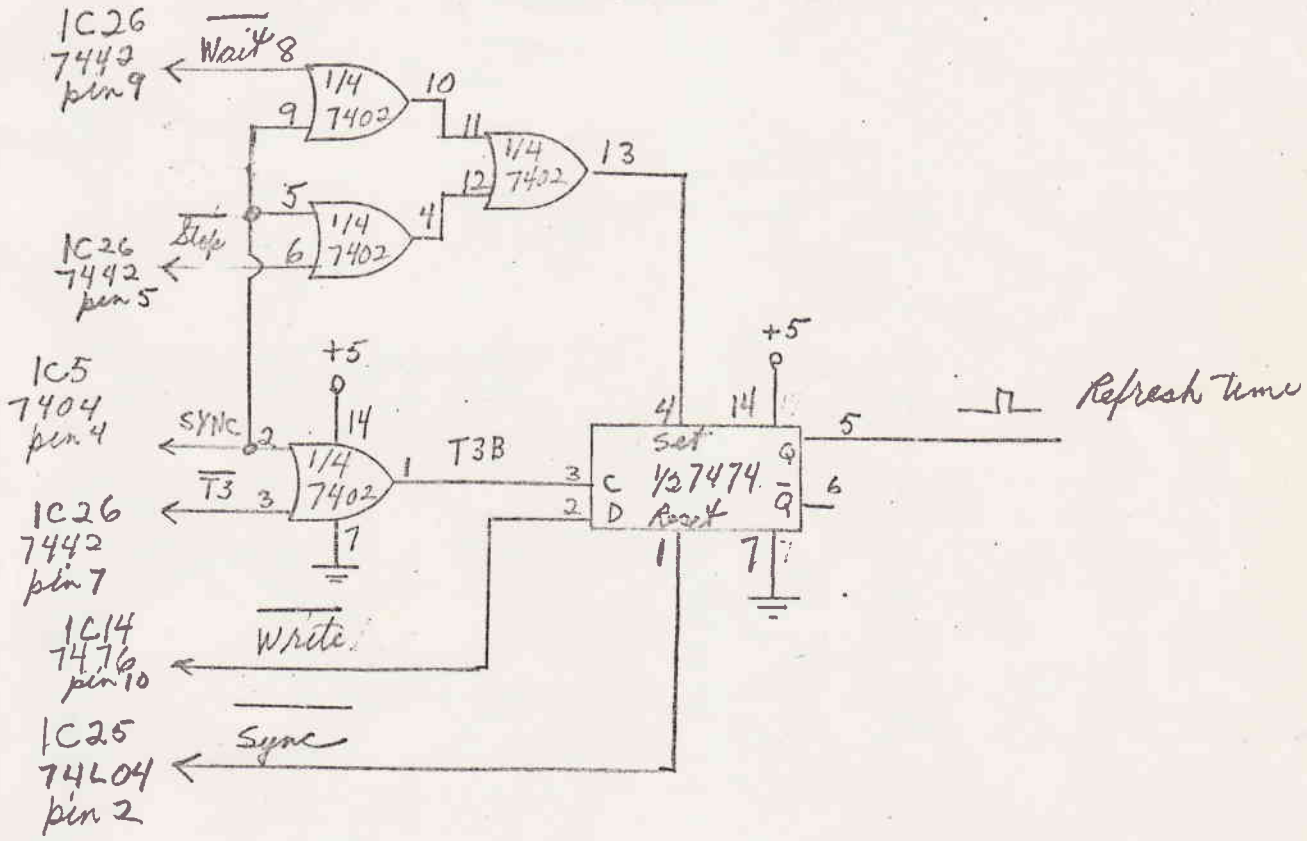
This small note is a sampling of the power requirements of Dr. Sudings Mark-8 Minicomputer, 1974.

The following pages show a few Mark-8 mods, and lead into the design of the Digital Group systems. There are pages detailing preliminary design of the "Suding buss", motherboard layout, some card circuitry, and the operating software. All of these documents are in the handwriting of Dr. Suding.

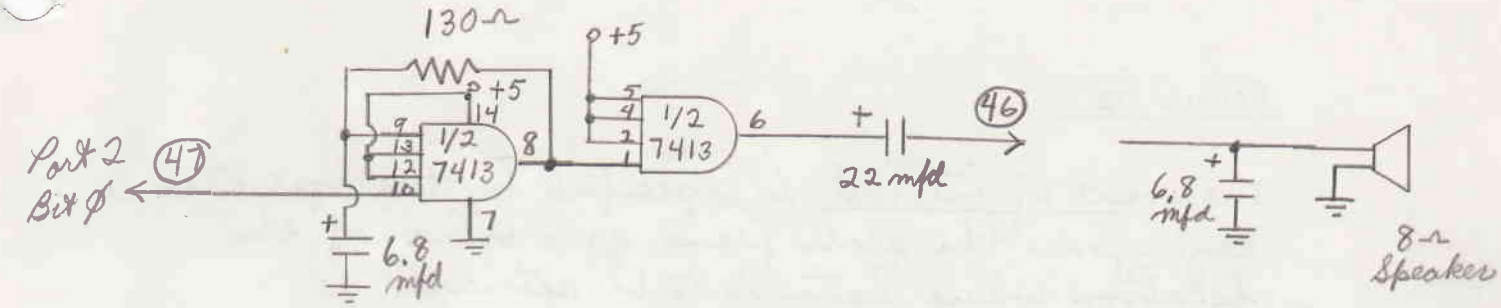
Mark 8 CPU board modifications

for 4K Dynamic RAM support

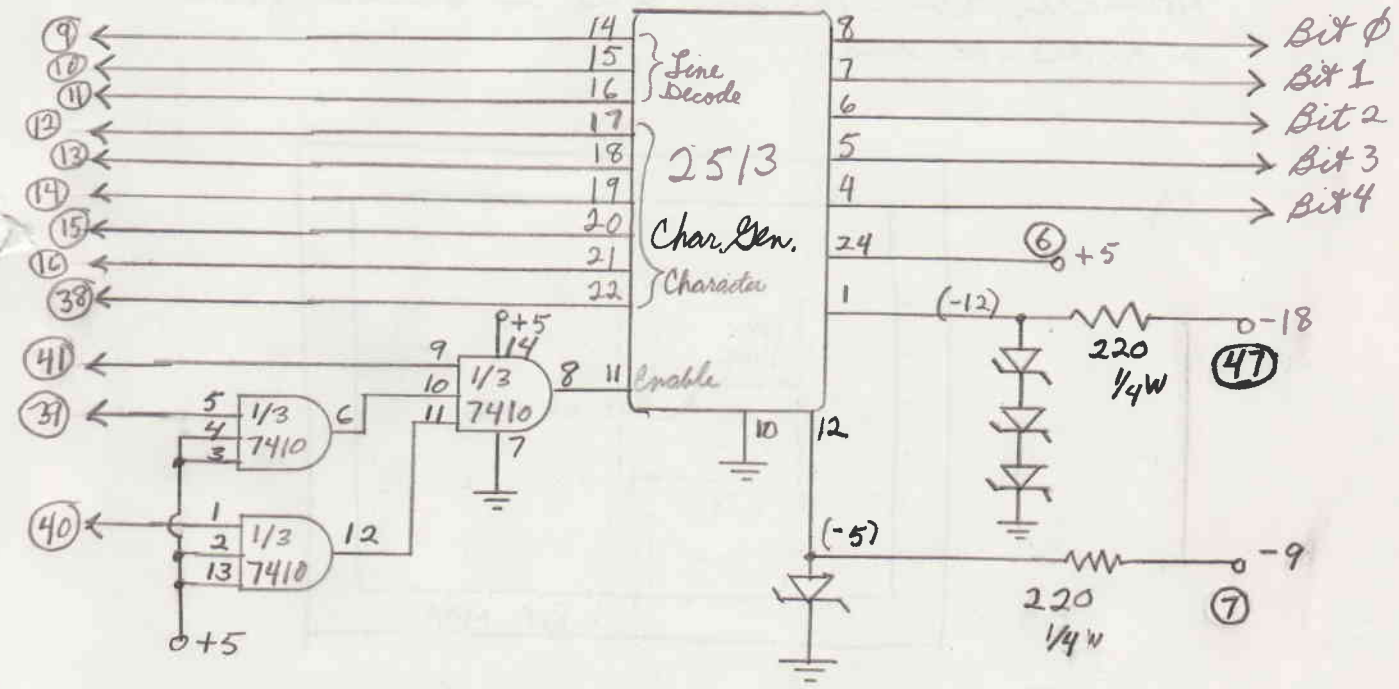
under cycle steal.



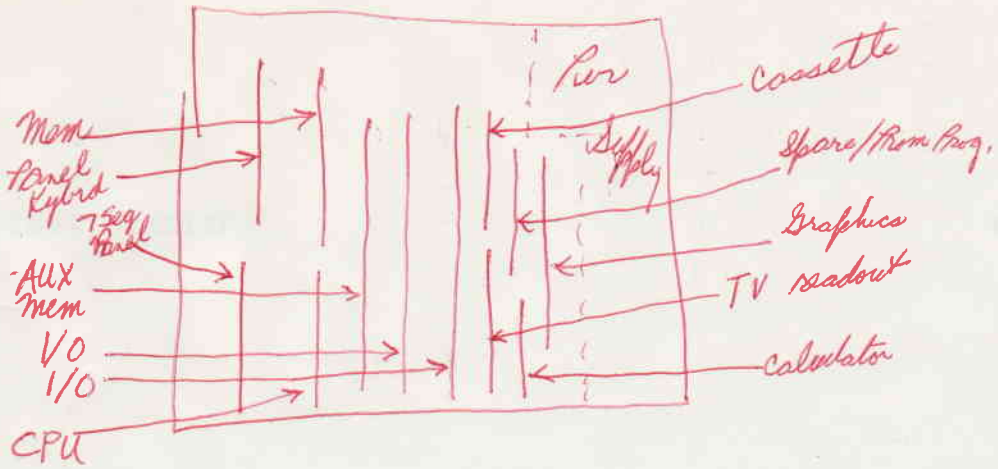
Special Mods.



CW Oscillator Mod (on CPU board)



Char Gen on Memory Board 2 – 2K-2.5K output



Pins

Graphics: (47 pin) (use -5 & wire direct)

⏚ = 3 +5 = 6 -12 = 7 +12 = 34

Byte 1 Bit 0 = 10, 1 = 11, 2 = 12, 3 = 13, 4 = 14, 5 = 15, 6 = 16, 7 = 17

Byte 2 Bit 0 = 36, 1 = 37, 2 = 38, 3 = 39, 4 = 40, 5 = 41, 6 = 42, 7 = 43

Video: B/W + Sync = 1 Color: Red = 27, 10 Blue = 25, 5 Green = 23, 4

Calculator (22 pin single)

⏚ = 1 -12 = 11 +12 = 13 +5 = 22

Input from CPU Bit 0 = 21, 1 = 20, 2 = 19, 3 = 18, 4 = 17, 5 = 16, 6 = 15, 7 = 14

Output to CPU Bit 0 = 12, 1 = 10, 2 = 9, 3 = 8, 4 = 7, 5 = 6, 6 = 5, 7 = 4

TV Readout (22 pin Single)

⏚ = 3 +5 = 6 -12 = 7 +12 = 11 Video = 1

Data In: Bit 0 = 15, 1 = 16, 2 = 17, 3 = 18, 4 = 19, 5 = 22, 6 = 21, msB = 20

Cassette (22 pin Single)

⏚ = 25 +5 = 12 -12 = 2 +12 = 9

Cassette to board (Read) = 8 CPU to board (Data in) = 11

Board to cassette (Record) = 7 Board to CPU (Data out) = 1

I/O

Dual (22 pin)

⏚ = 2 top +5 = 1 top & bottom

Data to CPU (Lsb-Msb) 10-3 top

Data from CPU (Lsb-Msb) 10-3 bottom

Strobe: Input = 11 top Output = 20 bottom

Addresses: LSB = 12 bottom
1 = 13 "
2 = 14 "
3 = 15 "
4 = 16 bottom
5 = 17 bottom
6 = 18 "
7 = 19 "
8 = 12 top
9 = 13 "
10 = 14 "
11 = 15 "
12 = 16 top
13 = 17 "
14 = 18 "
MSB = 19 "

Dual (36 pin)

Port(Ø)	Out (Lsb-Msb)	In (Lsb-Msb)
	1-8 bottom	1-8 top
Port(1)	10-17 bottom	10-17 top
Port(2)	19-26 bottom	19-26 top
Port(3)	28-35 bottom	28-35 top

AUX mem (47 pin)

[also temp mem board]

-5 = 5 ⏚ = 3 -12 = 7 +5 = 6 +12 = 8

Read Strobe = 4
Write Strobe = 2
Cycle Steal = 1

R/W - 26 → ⏚

Memory Address (65 K max) (Lower Page bits)
LSB = 9
1 = 10
2 = 11
3 = 12
4 = 13
5 = 14
6 = 15
7 = 16

(Pages)
8 = 38
9 = 39
10 = 40
11 = 41
12 = 42
13 = 43
14 = 44
MSB = 45

Data from Cpu
LSB = 25
1 = 24
2 = 23
3 = 22
4 = 21
5 = 20
6 = 19
MSB = 18

Data to CPU
LSB = 35
1 = 34
2 = 33
3 = 32
4 = 31
5 = 30
6 = 29
MSB = 28

CPU (Dual 50 pin)

-5 = 4 bottom ⏚ = 3 top & bottom -12 = 7 top & bot. +5 = 6 top & bot +12 = 8 top & bot

$\overline{\text{mem Read Strobe}}$ = 12 top
$\overline{\text{I/O Read Strobe}}$ = 12 bottom

$\overline{\text{mem Write Strobe}}$ = 5 top
$\overline{\text{I/O Write Strobe}}$ = 5 bottom

Interrupt = 4 top
Cycle Steal time = 9 bottom

DMA request = 17 top
DMA granted = 17 bottom

Run SW = 26 top
Step SW = 26 bottom

Running Ind = 27 top
Reset SW = 27 bottom

Memory Addresses — as AUX mem; top & bottom

Data from mem: 35-28 top Data to Mem: 25-18 top

Data from I/O: 35-28 bottom I/O Data to mem: 25-18 top

Cpu Wait = 36 top
Spare = 36 bottom

Cassette to Cpu = 46 top I/O Port 1, Bit Ø, Input = 47 top
Cpu to Cassette 46 bottom I/O Bit 1, Bit Ø, Output = 47 bottom

48, 49, 50, 37, top & bottom unassigned

Front Panel 7 Segment Readout

⏚ = 1 & 22, bottom +5 = 2 & 21, top Strobe/Lamptest = 3 & 12, top & bottom (no connection)

High Address LSB = 11 top, 1 = 10 ", 2 = 9 ", 3 = 8 top, 4 = 7 top, 5 = 6 ", 6 = 5 ", MSB = 4 top

Low Address LSB = 20 top, 1 = 19 ", 2 = 18 ", 3 = 17 ", 4 = 16 top, 5 = 15 ", 6 = 14 ", MSB = 13 "

Panel Keyboard LSB = 11 bottom, 1 = 10 ", 2 = 9 ", 3 = 8 ", 4 = 7 bottom, 5 = 6 ", 6 = 5 ", MSB = 4 "

Mem Data LSB = 21 bottom, 1 = 20 ", 2 = 19 ", 3 = 18 ", 4 = 17 bottom, 5 = 16 ", 6 = 15 ", MSB = 14 "

Entry Digit LED: MSB = 1 top 1 = 3 bottom LSB = 13 bottom

Front Panel Keyboard

⏚ = 3 top & bottom + 5 = 6 top & bottom
Speaker Out = 1 top

DMA Request = 8 bottom
DMA Grant = 10 bottom
Read Strobe = 12 bottom
Write Strobe = 14 bottom

Panel Keyboard to Circuit: Clear = 27 top, 0 = 28 ", 1 = 29 ", 2 = 30 ", 3 = 31 ", 4 = 32 ", 5 = 33 ", 6 = 34 ", 7 = 35 ", 8 = 36 ", 9 = 37 ", A = 38 ", B = 39 ", C = 40 ", D = 41 top, E = 42, F = 43, High = 44, Low = 45, Deposit = 46, Examine = 47

Common = 26 top

Entry Digit MSD = 50 bottom, 1 = 49 ", LSB = 48 "

Circuit to Memory/CPU:

Address: Low LSB = 16 bottom, 1 = 17 ", 2 = 18 ", 3 = 19 ", 4 = 20 ", 5 = 21 ", 6 = 22 ", MSB = 23 "

High LSB = 24 bottom, 1 = 25 ", 2 = 26 ", 3 = 27 ", 4 = 28 ", 5 = 29 ", 6 = 30 ", MSB = 31 "

Mem Data to Mem: LSB = 32 bottom, 1 = 33 ", 2 = 34 ", 3 = 35 ", 4 = 36 ", 5 = 37 ", 6 = 38 ", MSB = 39 "

Panel Data LSB = 40 bottom, 1 = 41 ", 2 = 42 ", 3 = 43 ", 4 = 44 ", 5 = 45 ", 6 = 46 ", MSB = 47 "

Make Voltage Lines Wide

I/O Buss → Dual 22 pin Connector

Top of Card		Bottom (pin side)	
1.	+5	1.	Spare Voltage
2.	⏚	2.	−5
3.	MSB	3.	MSB
4.		4.	
5.	Data to CPU	5.	Data from CPU
6.		6.	
7.		7.	
8.		8.	
9.		9.	
10.	LSB	10.	LSB
11.	Input Strobe	11.	Spare
12.	MSB-7	12.	LSB
13.	MSB-6	13.	LSB+1
14.	MSB-5	14.	LSB+2
15.	MSB-4	15.	LSB+3
16.	MSB-3	16.	LSB+4
17.	MSB-2	17.	LSB+5
18.	MSB-1	18.	LSB+6
19.	MSB	19.	LSB+7
20.	Spare	20.	~~Spare~~ Output Strobe
21.	Spare	21.	Spare
22.	+12	22.	−12

Port address lines

Make Voltage lines wide

Memory Buss → Dual 36 pin Connector

Top of Card		Bottom (pin side)	
1.	+5	1.	Spare Voltage (most likely: +15)
2.	⏚	2.	−5
3.	MSB	3.	MSB
4.		4.	
5.	Data to CPU	5.	Data from CPU
6.		6.	
7.		7.	
8.		8.	
9.		9.	
10.	LSB	10.	LSB
11.	Read Data	11.	Spare
12.	MSB−7	12.	LSB
13	⋮	13	⋮
14	⋮	14	⋮
15	⋮	15	⋮
16	⋮	16	⋮
17	⋮	17	⋮
18	⋮	18	⋮
19	MSB	19	LSB+7
		20.	Write Data
20.	Spare	21	Spare
21	Cycle Steal	22	DMA Grant
22	DMA Request	23	Spare
23	Interrupt Request	24	Step
24	Run	25	CPU status
25	CPU Status	26	
26		27	Wait Ack
27	Wait Request	28	Halt Ack
28	Halt Request	29	Spare Lines
29	Spare Lines	⋮	
⋮		35	
35			
36	+12	36	−12

Memory Address Lines

[Make Voltage lines wide]

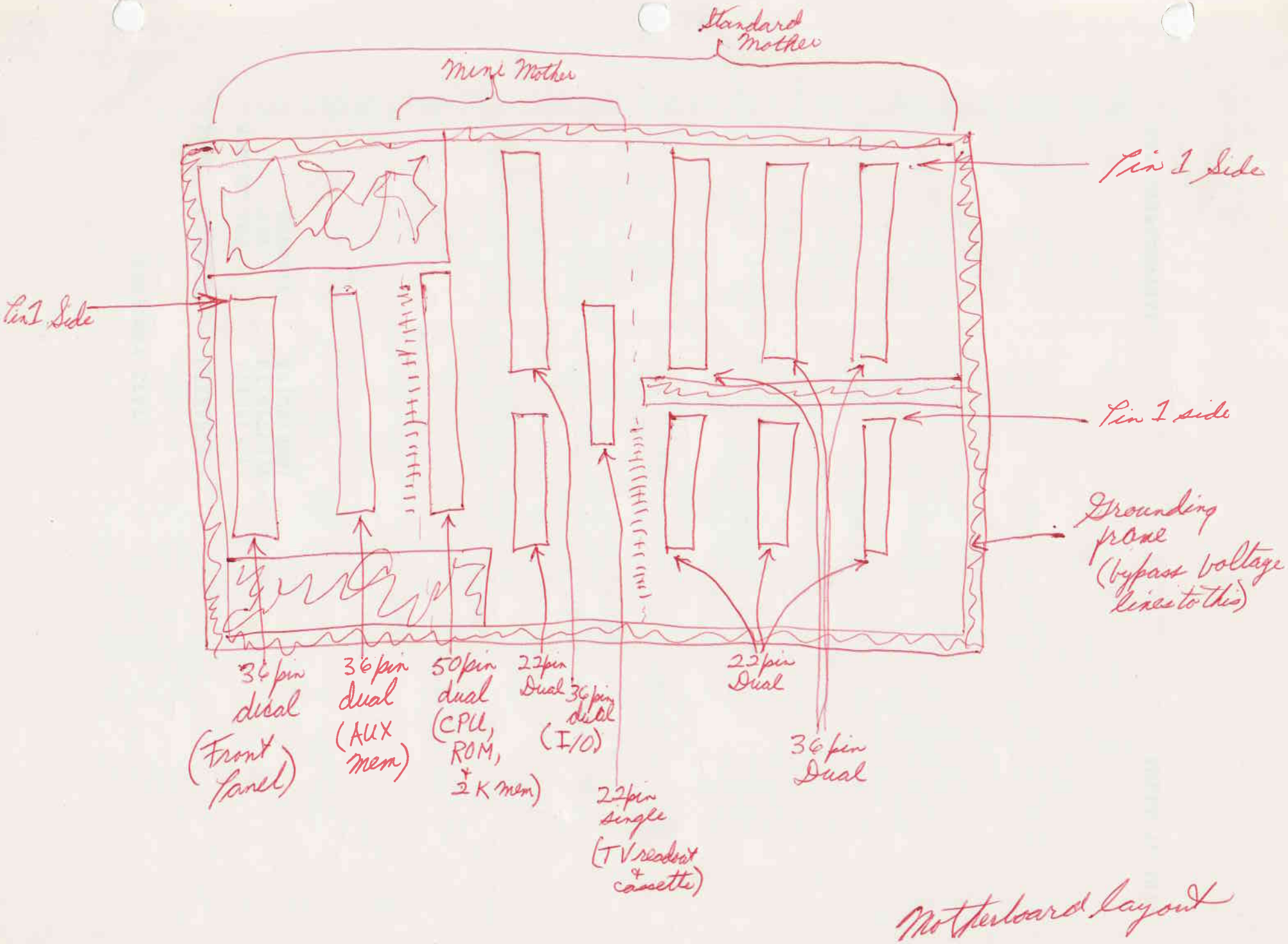
CPU Card → Dual 50 pin Connector

Top of Card - front		Bottom (pin side) - rear/I/O	
1.	+5	1.	+5
2.	⏚	2.	⏚
3.	Spare Voltage	3.	Spare Voltage
4.	-5	4.	-5
5,	MSB	5	MSB
6		6	
7	Data from memory	7	Data from I/O
8		8	
9		9	
10		10	
11		11	
12	LSB	12	LSB
13	MSB	13	MSB
14		14	
15	Data to memory	15	Data to I/O
16		16	
17		17	
18		18	
19		19	
20	LSB	20	LSB
21,	$\overline{\text{Mem}}$ Read Strobe	21.	I/O Read Strobe
22	LSB	22	LSB
23	⋮	23	⋮
24	memory address lines	24	Port address lines
25	⋮	25	⋮

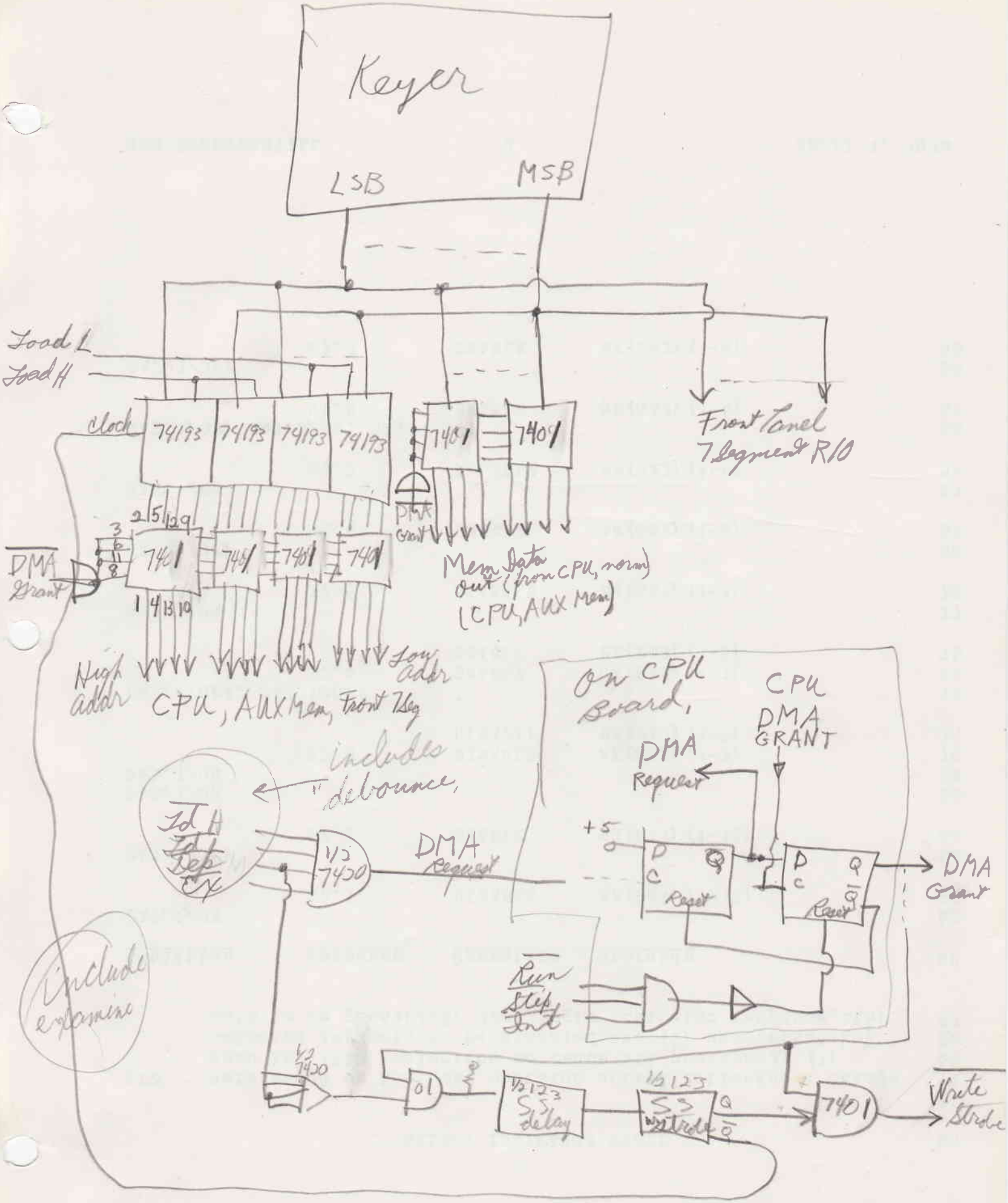
CPU cont.

Top of Card - front		Bottom (pin side) - rear / I/O	
26.		26.	
27.		27.	
28.		28.	
29.		29.	
30.		30.	
31.		31.	
32.		32	
33.		33.	
34.		34.	
35.		35	
36.		36	
37.	MSB	37.	MSB
38.	Memory Write Strobe	38.	I/O Write Strobe
39.	Cycle Steal	39.	Spare
40	DMA Request	40.	Data to Cassette Interface
41	DMA Grant	41.	I/O Port 1 out Bit Ø
42	Interrupt Request	42.	Data from Cassette Interface
43	Run	43.	I/O Port 1 Input Bit Ø
44	Step	44.	Spare
45	Wait	45.	Spare
46.	Wait acknowledge	46.	Spare
47	Halt	47.	Spare
48.	Halt acknowledge	48.	Spare
49.	+12	49.	+12
50.	-12	50.	-12

To be ~~[illegible]~~ used for both I/O & memory spare bus lines



Motherboard layout


Keyer
LSB
MSB
Load L
Load H
Clock
74193
74193
74193
74193
7401
7401
Front Panel
7 Segment R/O
DMA Grant
DMA Grant
Mem Data Out (from CPU, norm) (CPU, AUX Mem)
High addr
Low addr
CPU, AUX Mem, Front Seg
On CPU Board,
CPU DMA GRANT
DMA Request
+5
D
C
Q
Reset
DMA Grant
includes debounce,
Ld H
Ld
Step
Int
1/2 7400
DMA Request
Run
Step
Int
Include examine
1/2 7400
01
1/2 123 S.S. delay
1/2 123 S.S. Write
7401
Write Strobe

Major Ops

1 * Normal Entry & view
2 * Set Cursor on/off
3 * Space Fwd w/o write
4 * Backspace w/o write
5 * Home w/o write
6 * Read Data
7 * Read Horz Char address
8 * Read Line address
9 * Preset Horz address
10 * Preset Line address
11 * A/B page select
12 * Home Erase

Constraint

* Single I/O Port - 8 bits
* 512 Char — 32 x 16 format.

Impact of Major Ops on 512 Design

1. Disconnect the 7430 all bits home.
2. Fliplatch (2/4 7400), counter or osc (7493 or 7413), ~~Gate~~ (7430) Comparators (3-7485's)
3. Gate (1/4 7408) Up counter as 512 design
4. Gate (1/4 7408) Down counter (lift pin 4 & connect)
5. Reset 74193's (pin 14's)
6. MPXRs connected to 2102 outputs (4-74153's)
   MPXR outputs to CPU input port.
7. MPXRs connected to lower 5 bits of Write Clock Output
8. MPXRs connected to upper 4 bits of Write Clock Output
9. Selectors connected to lower 4 bits to Write Clock Reset
   " upper 5 bits to Write Clock Reset.
10.

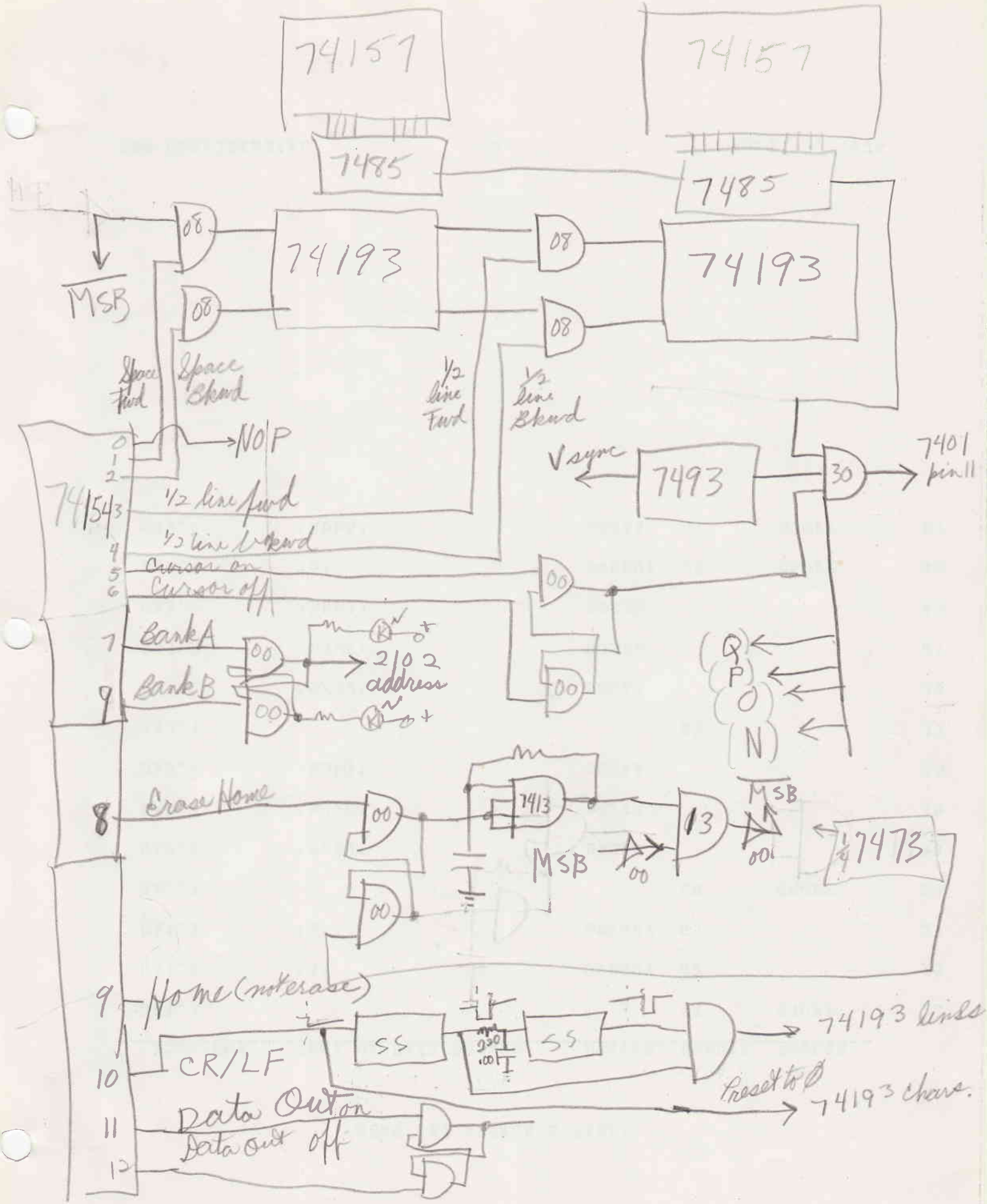
— Major problem area - not enough output data bits & selector bits. —

11. Fliplatch (2/4 7400) driving 2102's.
12. Erase (bit 6 high; others low) through double loop (Fliplatch - 2/4 7400 - pulse sel. - drives osc, driving the write clock, finally reset by pulse from "down the chain FF.) — Finally, #5 is invoked if necessary but may stop @ right spot.

Solution: 3 bits of address @ a time into latches
(4 2/4 - 7400's for latches)
(2 1/4 - 7432's for steering) Delayed Strobing (74123)

* also — upper 2 bits of #7 + #8 could be connected to A/B select & Cursor on/off for remote readout.

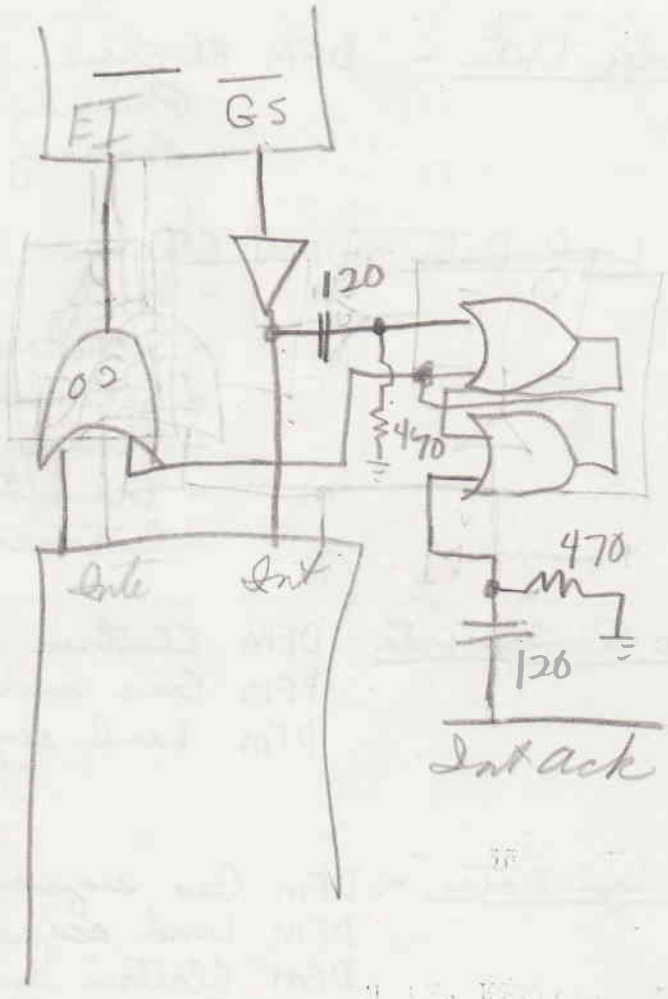
* Use 74154 as decoder; connect to 5 MSB of CPU output port.


74157
74157
7485
7485
74193
74193
08
08
08
08
MSB
Space Fwd
Space Bkwd
1/2 line Fwd
1/2 line Bkwd
NOP
74154
0
1
2
3
4
5
6
7
8
9
10
11
12
1/2 line fwd
1/2 line bkwd
Cursor on
Cursor off
Bank A
Bank B
00
2102 address
Erase Home
7413
13
MSB
7473
Home (not erase)
SS
SS
74193 lines
CR/LF
Preset to Ø
74193 chars.
Data Out on
Data out off
V sync
7493
30
7401 pin 11
Q
P
O
N

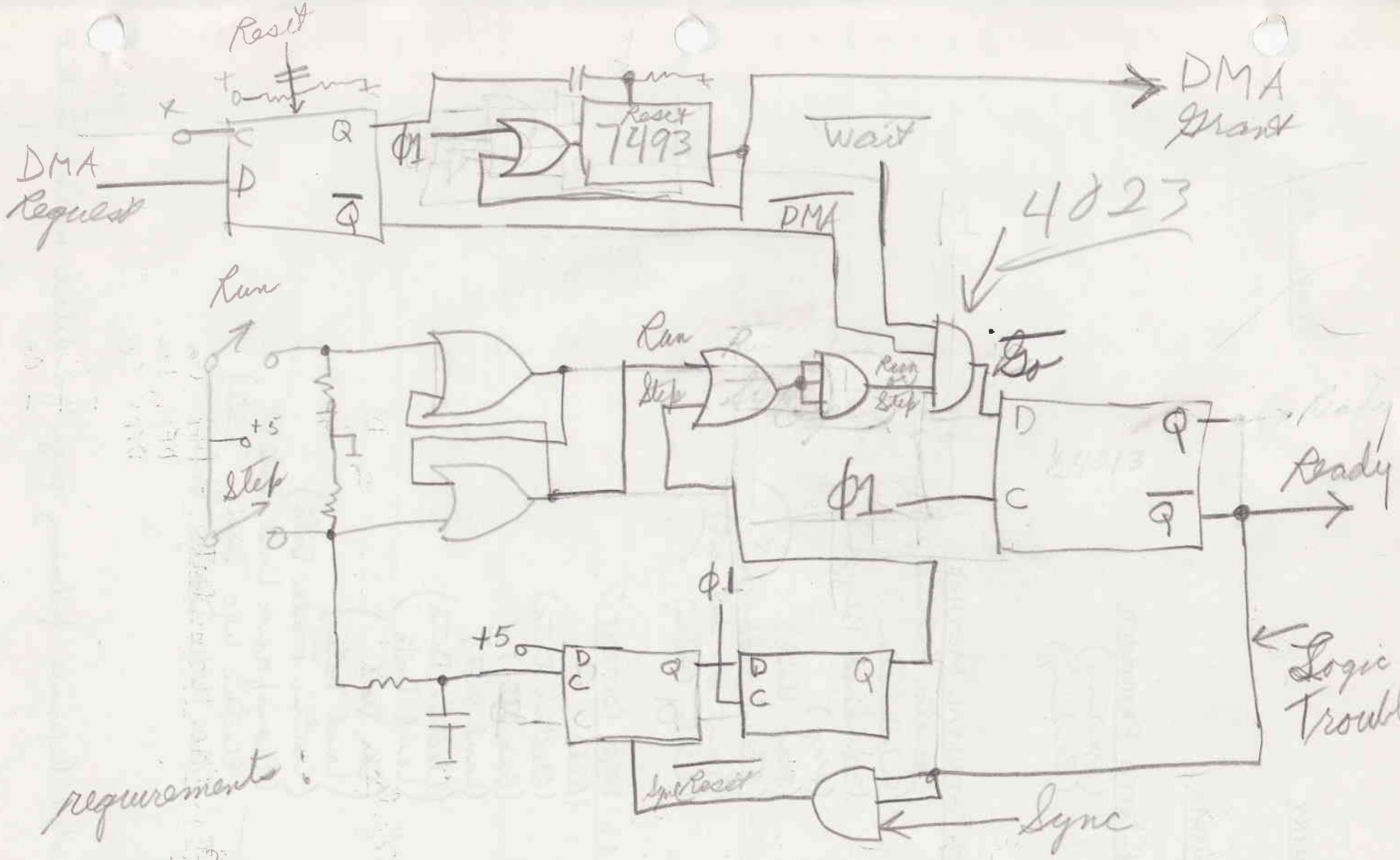
Problems:

Norm: * $\overline{GS}$ sets Int Latch,
* Inte comesback too fast & disables $\overline{EI}$,

With shorted $\overline{EI}$:
* $\overline{GS}$ up after $\overline{Intack}$ arises.



4
3
2
1
13
12
11
10

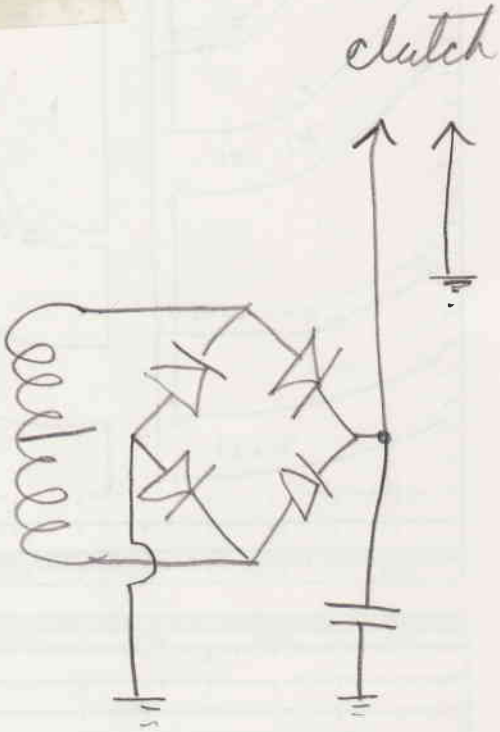


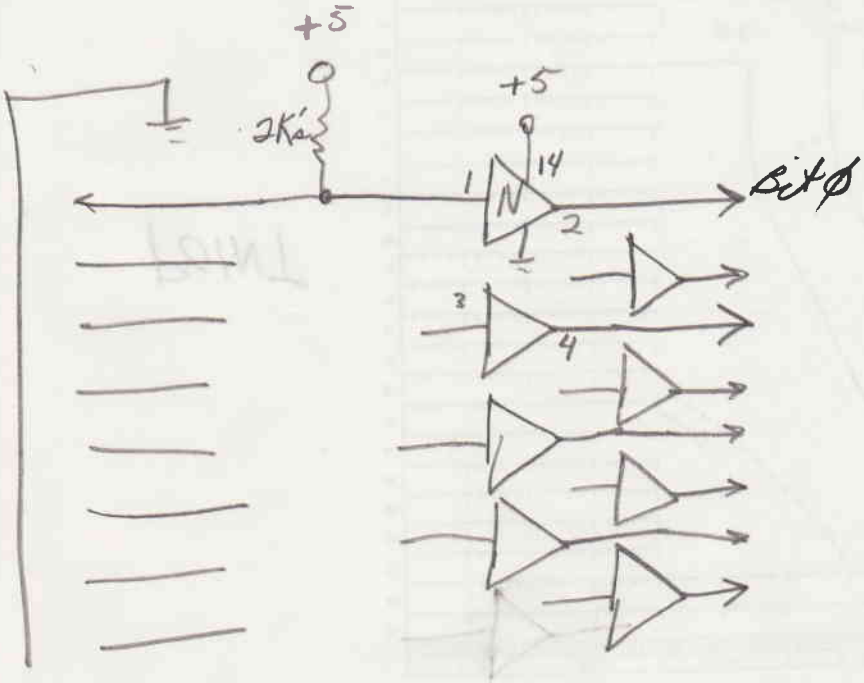
requirements:

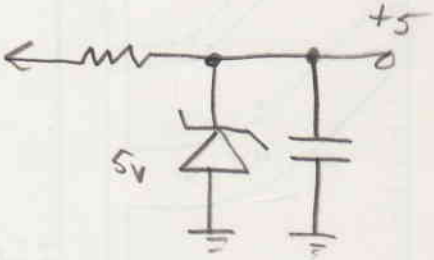
1 - 7402
2 - 7474 (4013?)
1 - 7410
1 - 7493
1 - 7400 buffer for $\phi 1$ & $\phi 2$

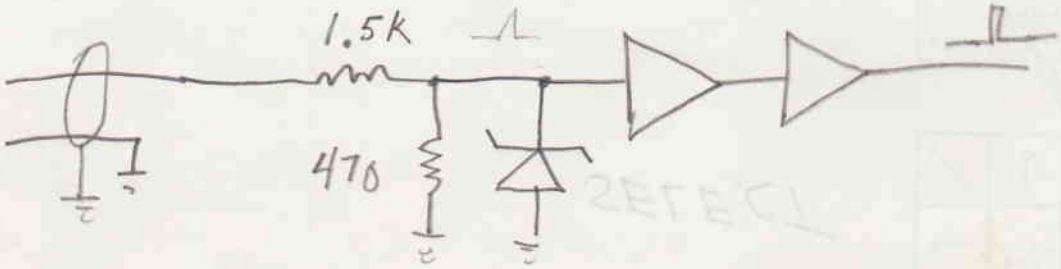
CMOS drive?
(Could use 4009 inv. buffer instead of 7400 or 4010 [non inv])


clutch
15
14
30
31
Pulse
34,35
FREE
13
STOP
RUN
33
29
Hold @ free
with tape on
16
28
Free
Stop
12
Run
18
7 6 5 4 3 2 1 8
10
free 1 2 3 4 5 6 7 8


clutch


+5
2Kω
+5
1
14
N
2
Bit Ø
3
4


+5
5v


1.5k
470

Cassette Interface Speed Test

	000	076	Load A with 000
	1	000	
(3)	2	006	Load B with XXX
	3	XXX	
(2)	4	016	Load C with 010
	5	010	
(1)	6	015	Decrement C
	7	302	Jump not zero (1)
	010	006	
	1	000	
	2	005	Decrement B
	3	302	Jump not zero (2)
	4	004	
	5	000	
	6	323	Out 1
	7	001	
	020	356	XOR A with 377
	1	377	(Invert A)
	2	303	Jump Uncondy (3)
	3	002	
	4	000	

Cassette	XXX				
000	007	=	2000	bits/sec	Look
010	010	=	1666	bits/sec	OK, Heavy rolloff
020	011	=	1538	bits/sec	OK, Considerable rolloff
030	012	=	1315	bits/sec	OK, Some Volume sens.
040	014	=	1176	bits/sec	OK, Rather full filtering
050	016	=	1000	bits/sec	OK, full sine wave
060	034	=	500	bits/sec	

3 pole low pass = .005, .01, .015

ASK II

006 012 076 215 315 030 006

006 000 303 ~~014~~ ~~006~~

005 302 004 006 311 000 000

000 000 000 000 000 000 000

000 000 000 365 305 345 366

006 030

200 376 212 312 113 006 376

215 302 067 006 315 117 006

076 015 315 117 006 076 012

315 117 006 303 113 006 376

241 322 101 006 076 240 303

006 077 110 006 376 340 332 110 006

346 337 315 117 006 341 301

361 311 346 117 046 011 247

027 365 346 001 323 002 361

315 156 006 037 045 302 125

006 076 001 323 002 315 156

006 315 156 006 311 016 034

006 067 005 302 162 006 015

302 160 006 311 000 000 000

006 176 000

Baudot

Motor On

Character

Motor off?

006 000	~~006~~	~~012~~	~~076~~	~~215~~			
	303	014	006	303	030	006	303
006 014				Forms Feed			
	000	005	303	014	006	006	005
	076	215	315	030	006	005	302
006 030							
	020	006	311	365	305	325	345
	366	200	376	212	312	173	006
	376	215	302	073	006	026	003
	076	010	315	210	006	025	302
	052	006	076	002	315	210	006
	303	173	006	376	241	322	105
	006	076	340	303	170	006	376
	340	332	114	006	326	040	376
006 115							
	300	332	137	006	365	072	263
	006	376	037	312	160	006	076
	037	303	152	006	365	072	263
	006	376	033	312	160	006	076
6151	033	062	263	006	315	210	006
	361	376	300	322	170	006	306
	100	315	200	006	341	321	301
	361	311	041	264	006	326	300
6205							